AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (currently amended) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

programming said programmable logic circuitry to function as communications port circuitry;

establishing with said programmed programmable logic circuitry a connection between ~~the~~ said integrated circuit chip and an ~~external~~ off-chip source of data for use in ~~configuring the~~ reprogramming said programmable logic circuitry;

transferring data from said ~~external~~ off-chip source to said integrated circuit chip using said connection; and

using transferred data to ~~configure the~~ reprogram said programmable logic circuitry to function as other than communications port circuitry.

2. (new) The method of claim 1 wherein said transferring data comprises transferring data from said off-chip source to a memory on said integrated circuit chip using said connection.

3. (new) The method of claim 1 wherein said programming comprises programming said programmable logic circuitry to function as Ethernet media access controller (MAC) circuitry.

4. (new) The method of claim 1 further comprising before said programming:

establishing a first connection between said integrated circuit chip and a first off-chip source of data for use in programming said programmable logic circuitry to function as communications port circuitry; and

transferring data for use in programming said programmable logic circuitry to function as communications port circuitry from said first off-chip source to said integrated circuit chip using said first connection.

5. (new) The method of claim 4 wherein said establishing a first connection comprises establishing with Ethernet MAC circuitry a first connection between said integrated circuit chip and a first off-chip source of data for use in programming said programmable logic circuitry to function as communications port circuitry.

6. (new) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry a connection between said integrated circuit chip and an off-chip source of data;

transferring data from said off-chip source to said integrated circuit chip using said connection;

programming Ethernet media access controller (MAC) circuitry with said transferred data;

establishing with said Ethernet MAC circuitry a second connection between said integrated circuit chip and a second off-chip source of data;

transferring data from said second off-chip source to said integrated circuit chip using said second connection; and

using transferred data from said second off-chip source to program said programmable logic circuitry.

7. (new) The method of claim 6 wherein said programming Ethernet MAC circuitry comprises programming Ethernet MAC circuitry with said transferred data indicating a speed of operation at which said Ethernet MAC circuitry is to operate.

8. (new) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising:

establishing with receiver/transmitter circuitry a connection between said chip and an off-chip source of data;

transferring data from said off-chip source to said chip using said connection;

programming said programmable logic circuitry with said transferred data to function as Ethernet media access controller (MAC) circuitry;

establishing with said programmed programmable logic circuitry a second connection between said integrated circuit chip and a second off-chip source of data;

transferring data from said second off-chip source to said integrated circuit chip using said second connection; and

using transferred data to reprogram said programmable logic circuitry to function as something other than said Ethernet MAC circuitry.

9. (new) An integrated circuit chip comprising:

programmable logic circuitry;

processor circuitry operative to program said programmable logic circuitry; and

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data, said Ethernet MAC circuitry coupled to said processor circuitry.

10. (new) The integrated circuit chip of claim 9 wherein said processor circuitry is microprocessor circuitry.

11. (new) The integrated circuit chip of claim 9 wherein said programmable logic circuitry is reprogrammable.

12. (new) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 9; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

13. (new) The end-user system of claim 12 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

14. (new) The end-user system of claim 12 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated

circuit chip operative to establish a connection to said source.

15. (new) The end-user system of claim 12 wherein said end-user system comprises a data processing system.

16. (new) A circuit board on which is mounted an integrated circuit chip as defined in claim 9.

17. (new) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry;

processor circuitry operative to program said programmable logic circuitry;

memory circuitry;

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data; and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, memory circuitry, and Ethernet MAC circuitry.

18. (new) The integrated circuit chip of claim 17 wherein said processor circuitry comprises a central processor unit.

19. (new) The integrated circuit chip of claim 17 wherein said processor circuitry is microprocessor circuitry.

20. (new) The integrated circuit chip of claim 17 wherein said memory circuitry is random access memory (RAM).

21. (new) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 17; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

22. (new) The end-user system of claim 21 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

23. (new) The end-user system of claim 21 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

24. (new) The end-user system of claim 21 wherein said end-user system comprises a data processing system.

25. (new) A circuit board on which is mounted an integrated circuit chip as defined in claim 17.

26. (new) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry;

processor circuitry operative to program said programmable logic circuitry;

receiver/transmitter circuitry;

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data; and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, receiver/transmitter circuitry, and Ethernet MAC circuitry.

27. (new) The integrated circuit chip of claim 26 wherein said programmable logic circuitry is operative to be selectively reprogrammed.

28. (new) The integrated circuit chip of claim 26 further comprising memory circuitry wherein said processor circuitry is operative to program said programmable logic circuitry with data stored in said memory circuitry.

29. (new) The integrated circuit chip of claim 26 wherein said memory is a random access memory (RAM).

30. (new) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 26; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

31. (new) The end-user system of claim 30 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

32. (new) The end-user system of claim 30 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

33. (new) The end-user system of claim 30 wherein said end-user system comprises a data processing system.

34. (new) A circuit board on which is mounted an integrated circuit chip as defined in claim 26.

35. (new) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as Ethernet media access controller (MAC) circuitry;

processing circuitry operative to program said programmable logic circuitry;

receiver/transmitter circuitry; and

interconnection bus circuitry coupled to said programmable logic circuitry, processing circuitry, and receiver/transmitter circuitry.

36. (new) An end-user system comprising:

a circuit board comprising:

a processor;

a memory;

I/O circuitry;

an integrated circuit chip as defined in claim 35; and

a system bus coupling said processor, memory, I/O circuitry, and integrated circuit chip.

37. (new) The end-user system of claim 36 further comprising a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

38. (new) The end-user system of claim 36 wherein said circuit board further comprises a source of configuration data for said programmable logic circuitry, said integrated circuit chip operative to establish a connection to said source.

39. (new) The end-user system of claim 36 wherein said end-user system comprises a data processing system.

40. (new) A circuit board on which is mounted an integrated circuit chip as defined in claim 35.